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09/932,113	08/20/2001	Hiroshi Kageyama	500.40528X00	4240

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,113	KAGEYAMA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-16 and 25-30* is/are rejected.

7)☐ Claim(s) *4-8,17-24,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 1, 3, 10, 12-16, 28, 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiraki et al. (US Patent No. 6,504,522 B2).

As to claim 1, Shiraki et al. teaches an image display apparatus (See Col. 1, Lines 14-16) comprising:

image display means including a pixel in a region near an intersection at which each of signal lines and each of scanning lines are intersected each other (See Fig.2, items SL1, GL1, 10, Col. 7, Lines 6-16), said signal lines and said scanning lines being arranged in a matrix shape (See Fig. 2, item 1), and said pixel being connected to said signal line and said scanning line via an switch element (See Fig. 3, items SL, GL, SW, Col. 7, Lines 16-20);

a group of gradation voltage lines applied analogue gradation voltages in accordance with display gradations (See Fig. 1, items V1-V8, from Col. 7, Line 66 to Col. 8, Line 8);

decoder means for producing switch drive signals by which any one of said gradation voltage lines is selected in accordance with digital high-gradation image data (See Fig. 1, item 13, Col. 8, Lines 30-39);

trigger signal output (in the reference are equivalent to output Q1-Q3) means for sequentially producing trigger signals in accordance with said image data (See Fig. 1, items 11-12, Q and Fig. 4, items Q1-Q3 Col. 8, Lines 16-22); and

a plurality of switch means for selecting a specified gradation voltage line in response said switch drive signals under condition in which said trigger signals are inputted, to supply a gradation voltage from said specified gradation voltage line to specified signal line See Fig. 1, items 14a-14h, SL, Col. 8, Lines 30-39).

As to claim 3, Shiraki et al. teaches a plurality of switch drive lines for transmitting said switch drive signals are connected to said decoder means (See Fig. 1, items ASW1-ASW8, Col. 8, Lines 30-39);

a plurality of trigger lines for transmitting said trigger signals are connected to said trigger signal output means (See Fig. 1, items Q1-Q3, Col. 8, Lines 16-22); and

output lines for transmitting said specified gradation voltage to said specified signal line are connected to said plurality of switch means (See Fig. 1-2, item SL, SL1-SL4, Col. 7, Lines 20-28).

As to claim 10, Shiraki et al. teaches output line is the same signal line (See Fig. 1-2, item SL, SL1-SL4, Col. 7, Lines 20-28).

As to claim 12, Shiraki et al. teaches when n is a display gradation number, a wiring number of group of gradation voltage lines is in range from n to 2 to the power n (See Fig. 1, items DAT1-DAT3, V1-V8).

As to claims 13-15, Shiraki et al. teaches image display means, said group of gradation voltage lines, decoder means, said plurality of switch means and said trigger signal output means are formed on a same substrate (See Fig. 1, items 11-14 and Fig. 2, items 2, 7, col. 6, Lines 56-65).

As to claim 16, Shiraki et al. teaches trigger signal output means is formed using a shift register (scanning) circuit (See Fig. 1, item 11, Col. 8, Lines 9-15).

As to claim 28, Shiraki et al. teaches each of pixel includes a liquid crystal interposed between a pair of substrates including transparent insulating substrate (See Fig. 3, item Cp); and

a light transmission factor of liquid crystal is changed in accordance with a voltage fed from switch element connected to pixel (See Fig. 3, item Cp, Col. 7, Lines 15-44).

As to claim 30, Shiraki et al. teaches scanning means for sequentially supplying scanning pulses to plurality scanning lines (See Fig. 2, items 3, GL1-GL3, Col. 7, Lines 5-14).

2. Claims 2, 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki et al. as applied to claim 1 above, and further in view of Callahan et al. (US Patent No. 5,726,676).

As to claim 2, Shiraki et al. does not show decoder means is divided into a plurality of decoders which are arranged to oppose each other.

Callahan et al. teaches decoder means is divided into a plurality of decoders which are arranged to oppose each other (See Fig. 2, item 14 and Fig. 3, item 30, Col. 2, Lines 6-17).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Callahan et al. into Shiraki et al. system in order to produce a great number of discrete analog voltage levels, while dissipating less power, and consuming less chip area (See Col. 1, Lines 55-58 in the Callahan et al. reference).

As to claims 25-26, Shiraki et al. does not show voltage generation means for applying different voltages to the group of gradation voltage lines, including plurality of ladder resistors connected in series with a voltage source.

Callahan et al. teaches voltage generation means for applying different voltages to the group of gradation voltage lines, including plurality of ladder resistors connected in series with a voltage source (See Fig. 3D, items Vo-V1, 37, Col. 9, Lines 47-64).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Callahan et al. into Shiraki et al. system in order to produce a great number of discrete analog voltage levels, while dissipating less power, and consuming less chip area (See Col. 1, Lines 55-58 in the Callahan et al. reference).

As to claim 27, Shiraki et al. teaches voltage generation means is formed on a same substrate as image display means, said group of gradation voltage lines, decoder

means, said plurality of switch means and said trigger signal output means are formed on a same substrate (See Fig. 1, items 11-14 and Fig. 2, items 2, 7, col. 6, Lines 56-65).

3. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki et al. as applied to claim 3 above, and further in view of Kosegawa et al. (US Patent No. 6,028,580).

Shiraki et al. does not show plurality of trigger lines and output lines are formed as a same wiring layer.

Kosegawa et al. teaches plurality of trigger lines (shift register output lines) and output lines are formed as a same wiring layer (See Fig. 14, items 65-66, Col. 2,Lines 21-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Kosegawa et al. into Shiraki et al. system in order to provide driving circuit (See Col. 1, Lines 5-9 in the Kosegawa et al. reference).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki et al. and Kosegawa et al. as applied to claim 9 above, and further in view of Koyama et al. (US Patent No. 6,549,184 B1).

Shiraki et al. and Kosegawa et al. do not show group of gradation voltage lines and plurality of switch drive lines are made of a wiring material of aluminum or copper.

Koyama et al. teaches aluminum as material for wiring lines (See Fig. 8, items 817-824, Col. 9, Lines 27-41).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Koyama et al. into Shiraki et al. and Kosegawa et al. system in order to obtain an excellent picture with high resolution (See Col. 2, Lines 32-33 in the Koyama et al. reference).

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraki et al. as applied to claim 1 above, and further in view of Dawson et al. (US Patent No. 6,307,322 B1).

Shiraki et al. does not show each of pixels includes a light emitting film formed on insulating substrate; and

a light emission intensity of light emitting film is changed in accordance with a voltage from switch element connected to pixel.

Dawson et al. teaches each of pixels includes a light emitting film formed on insulating substrate (See Fig. 1, item 106, Col. 3, Lines 52-65);

a light emission intensity of light emitting film is changed in accordance with a voltage from switch element connected to pixel (See Fig. 1, item 106, from Col. 3, Line 66 to Col. 4, Line 8).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teaching of Dawson et al. into Shiraki et al. system in order to reduce sensitivity to the threshold variations (See Col. 1, Lines 55-58 in the Callahan et al. reference).

Allowable Subject Matter

6. Claims 4-8, 17-24, 31-32 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

Relative to claim 4, the major difference between the teaching of the prior art of record (Shiraki et al., Kosegawa et al. and Koyama et al.) and the instant invention is that the said prior art **does not teach** plurality of switch drive lines and group of gradation voltage lines are arranged to intersect plurality of trigger lines and output lines as related to particular layout.

Claims 5-7 depend on claim 4.

Relative to claim 8, the major difference between the teaching of the prior art of record (Shiraki et al., Kosegawa et al. and Koyama et al.) and the instant invention is that the said prior art **does not teach** group of gradation voltage lines and plurality of switch drive lines are formed as a same wiring layer, as related to particular layout.

Relative to claim 17, the major difference between the teaching of the prior art of record (Shiraki et al., Kosegawa et al. and Koyama et al.) and the instant invention is that the said prior art **does not teach** each of plurality of switch means includes:

a first thin film transistor which becomes which becomes conductive by being inputted said trigger signal to transmit said switch drive signal; and

a second thin film transistor which becomes conductive by said switch drive signal produced from a first thin film transistor to transmit a gradation voltage to said output line.

Claims 18-24 depend on claim 17.

Relative to claim 31, the major difference between the teaching of the prior art of record (Shiraki et al., Kosegawa et al. and Koyama et al.) and the instant invention is that the said prior art **does teach** when said image display apparatus is driven, a drive frequency at which said switch drive signals are supplied from said decoder means to said plurality of switch drive lines is set to twice or more as high as a drive frequency at which said trigger signals are supplied **from said trigger signal output means.**

Claim 32 depends on claim 31.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 02.28.05

VIJAY SHANKAR
PRIMARY EXAMINER